CLAIMS

What is claimed is:

1. A magnetic random access memory array comprising:

a plurality of magnetic storage cells;

a plurality of global word lines;

a plurality of magnetic word lines, each of the plurality of magnetic word lines having a plurality of segments, each of the plurality of segments being coupled with at least one of the plurality of global word lines such that each of the plurality of segments is separately selectable, each of the plurality of segments being coupled to a portion of the plurality of magnetic storage cells;

a plurality of read bit lines oriented at an angle with respect to the plurality of magnetic word lines;

a plurality of selection devices, the plurality of read bit lines being coupled with the plurality of magnetic cells through the plurality of selection devices; and

a plurality of write bit lines substantially parallel to the plurality of read bit lines.

2. The magnetic random access memory array of claim 1 wherein the plurality of magnetic storage cells further includes:

a plurality of magnetic tunneling junctions, each of the magnetic tunneling junctions including a free layer and a pinned layer separated by an insulator layer, each of the plurality of magnetic tunneling junctions being in direct electrical contact with a segment of the

plurality of segments.

3. The magnetic random access memory array of claim 2 wherein the segment is separated from the free layer of the magnetic tunnel junction element by at least one conducting non-magnetic spacer layer.

4. The magnetic random access memory array of claim 3 wherein the at least one conducting non-magnetic spacer layer has a thickness of 300 angstroms or less.

5. The magnetic random access memory array of claim 1 wherein the plurality of global word lines has a lower line resistance than the plurality of magnetic word lines.

6. The magnetic random access memory array of claim 1 wherein the plurality of global word lines is oriented substantially parallel to the plurality of magnetic word lines.

7. The magnetic random access memory array of claim 1 wherein the plurality of selection devices include a plurality of selection transistors.

8. The magnetic random access memory array of claim 1 wherein the plurality of read bit lines are connected to the plurality of magnetic storage cells through diodes.

9. A method for utilizing a magnetic random access memory array having a plurality of magnetic storage cells, a plurality of global word lines, and a plurality of magnetic word lines having a plurality of segments, each of the plurality of segments being coupled with at least one of the plurality of global word lines such that each of the plurality of segments is separately selectable, the method comprising the steps of:

(a) in the write mode, driving a current through at lest one of the plurality of global word lines;

(b) in the write mode, selecting at least one of the plurality of segments;

(d) in the write mode, providing a first write current through the at least one of the plurality of segments; and

(e) in the write mode, providing a second write current to a plurality of write bit lines;

wherein the plurality of magnetic storage cells are coupled with a plurality of read bit lines through the plurality of selection devices, the plurality of read bit lines being oriented at an angle with respect to the plurality of magnetic word lines.

10. The method of claim 9 further comprising the steps of:

(f) in a read mode, grounding a global word line, the read mode for reading a portion of the plurality of magnetic storage device, the portion of the plurality of magnetic storage cells including more than one storage cell;

(g) in the read mode, providing a read current in a portion of the plurality of read

bit lines;

(h) in the read mode, activating a portion of the plurality of selection devices; and

(i) in the read mode, reading a voltage across a portion of the plurality magnetic elements.

11. The method of claim 9 wherein the plurality of magnetic storage cells further includes a plurality of magnetic tunneling junctions, each of the magnetic tunneling junctions including a free layer and a pinned layer separated by an insulator layer, each of the plurality of magnetic tunneling junctions being in direct electrical contact with a segment of the plurality of segments.

12. The method of claim 11 wherein the segment is separated from the free layer of the magnetic tunnel junction element by at least one conducting non-magnetic spacer layer.

13. The method of claim 12 wherein the at least one conducting non-magnetic spacer layer has a thickness of 300 angstroms or less.

14. The method of claim 9 wherein the plurality of global word lines has a lower line resistance than the plurality of magnetic word lines.

15. The method of claim 9 wherein the plurality of global word lines is oriented substantially parallel to the plurality of magnetic word lines.

16. The method of claim 9 wherein the plurality of selection devices include plurality of selection transistors.

17. The method of claim 9 wherein the plurality of read bit lines are connected to the plurality of magnetic storage cells through diodes.